UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,037	06/19/2003	Hannu Huotari	ASMMC.047AUS	8258

20995 7590 02/18/2004

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,037	HUOTARI, HANNU	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the communication filed June 19, 2003.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "750" (paragraph 0054). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-24, 27, 28, 33-38 and 40-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Bai et al. (US 6,166,417).

Regarding claim 1, Bai discloses a gate stack in an integrated circuit having PMOS and NMOS regions, a dielectric layer (120), and a barrier layer (125) that overlies both the PMOS and NMOS regions (Fig. 2 and 9; col. 3, ln. 6-35).

Regarding claims 2, 3, 23 and 24, Bai discloses that the barrier layer may be TiN or TaN, both of which are conductive material (col. 3, ln. 51-54).

Regarding claims 5, 6, 27 and 28, Bai discloses that the barrier layer has a thickness of 5 – 200 ´ (col. 3, ln. 36-37).

Regarding claim 7, Bai discloses that the gate stack includes a first gate electrode layer (130 or 135) and a second gate electrode layer (130 or 135) (col. 3, ln. 55-65; col. 4, ln. 41-53).

Regarding claims 8 and 17, Bai discloses the first and second gate electrode layers are adjacent (Fig. 7).

Regarding claims 9 and 18, Bai discloses that the first gate electrode layer includes a first gate electrode material and the second gate electrode includes a second gate electrode material (col. 3, ln. 55-65; col. 4, ln. 41-53).

Regarding claims 10, 11, 19 and 20, Bai discloses that if the first gate electrode is made of N-type material, the second electrode will be made of P-type material, and vice-versa. The first gate electrode material may include nickel or ruthenium oxide if the material is to have the work function of a P-type doped semiconductor or may include ruthenium if the material is to have the work function of an N-type doped semiconductor. The same is true for the second gate electrode. Hence, the first and second gate electrodes will be made of different conductive materials. See col. 1, ln. 42-54; col. 3, ln. 55 – col. 4, ln. 9; col. 4, ln. 41-53).

Regarding claim 12, Bai discloses that the first gate electrode may overlie the PMOS region (115) and the second gate electrode may overlie the NMOS region (105) (col. 3, ln. 1-16; col. 4, ln. 4-9).

Regarding claims 13 and 14, Bai discloses that the work functions of both the first and second gate electrodes is determined by the materials (130/135) of the first and second gate electrodes (col. 3, ln. 48-51).

Regarding claim 15, Bai discloses depositing a dielectric layer (120) over first and second regions (105/115) of a substrate, depositing a barrier layer (125) directly over the dielectric layer such that it overlies both the first and second regions, and forming first and second gate electrode layers (130/135) over the first -and second regions, respectively (col. 3, ln. 17 - col. 4, ln. 64).

Regarding claim 16, Bai discloses that one of the regions is a PMOS region and the other region is an NMOS region (col. 3, ln. 8-16).

Regarding claim 21, Bai discloses that the first and second gate electrode materials may be made of nickel, ruthenium oxide or ruthenium (col. 1, ln. 41-53; col. 4, ln. 3-9; col. 4, ln. 42-53).

Regarding claim 22, Bai discloses that one of the gate electrodes may be made of a metal nitride (MoN) (col. 1, ln. 41-53).

Regarding claim 33, Bai discloses depositing a layer of first gate electrode material (130 or 135 can be considered "a first gate electrode layer") over the first and second regions of the substrate (Fig. 4 and 6).

Regarding claim 34, Bai discloses removing the first gate electrode material from over the second region without removing the underlying barrier layer (Fig. 5 and 7).

Regarding claim 35, in the event that the material 135 is considered to be the first gate electrode material, Bai discloses that the first gate electrode material is removed from over the second region by chemical mechanical polishing (col. 4, ln. 55-64).

Regarding claim 36, Bai discloses depositing a layer of second gate electrode material (130 or 135 can be considered "a second gate electrode layer") over the first and second regions of the substrate (Fig. 4 and 6).

Regarding claim 37, in the even that the material 130 is considered to be the first gate electrode material, Bai discloses that the first gate electrode material is removed from over the second region by differential etching (col. 29-33).

Regarding claims 38 and 41, Bai discloses depositing a layer of second gate electrode material (130 or 135 can be considered "a second gate electrode layer") over the first and second regions of the substrate and removing the second gate electrode material from over the first region without removing the underlying barrier layer (Fig. 5, 7 and 8).

Regarding claim 40, Bai discloses etching the barrier layer over portions of the second region to a thickness of 0 Angstroms (Fig. 8).

Regarding claim 42, Bai discloses depositing a dielectric layer (120) over first and second regions (105/115) of a substrate, depositing a barrier layer (125) directly over the dielectric layer such that it overlies both the first and second regions, depositing a first gate electrode material (130 or 135) over the first and second regions, removing the first gate electrode material from over the first region without removing the barrier layer, depositing a second gate electrode material (135 or 130), and defining a first and second electrode in the first and second regions.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (US 6,166,417) in view of Elers et al. (WO 01/29893 A1).

Regarding claims 4, 25 and 26, Bai does not disclose that the barrier layer is a nanolaminate; nor does Bai discloses by what method the barrier layer may be deposited. Like Bai, Elers discloses depositing a barrier layer onto a layer of SiO_2 dielectric. Elers states that it is advantageous to form barrier layers such that they are nanolaminates because nanolaminates "have enhanced diffusion barrier properties" by virtue of their structure having "very complicated diffusion paths for impurities through disruption of normal crystal growth during deposition" (pg. 8, ln. 20-25). The nanolaminate barrier layer is formed by an ALD (atomic layer deposition process) (pg. 1, ln. 28-32). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the barrier layer of Bai such that it is a nanolaminate deposited by ALD because Elers teaches that a nanolaminate structure provides enhanced diffusion barrier properties and Elers teaches that ALD is the way in which such a structure is created.

Claims 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (US 6,166,417) in view of Elers et al. (WO 01/29893 A1) and Pomarede et al. (US 6,613,695).

Regarding claims 29-32, Bai discloses that the gate dielectric layer may be SiO_2, but Bai does not disclose a method of forming the dielectric layer, nor treating the dielectric layer to remove OH groups. As discussed above in reference to claims 4, 25 and 26, in view of the teachings of Elers, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form the barrier layer of Bai by the ALD nanolaminate process of Elers in order to improve the diffusion barrier properties of the barrier layer. Pomarede teaches that it is

advantageous to treat a layer such as SiO_2 with a mixture including ammonia (nitrogen-hydrogen) plasma and nitrogen radicals in the event that the SiO_2 layer will be covered with a layer of material deposited by ALD (col. 8, ln. 61 – col. 9, ln. 35). This process inherently replaces OH groups on the surface of the SiO_2 with nitrogen atoms. Pomarede states, "By changing the surface termination of the substrate [SiO_2] with a low temperature radical treatment, subsequent deposition is advantageously facilitated without significantly affecting the bulk properties of the underlying material." (Abstract). At the time of the invention, it would have been obvious to one of ordinary skill in the art to treat the surface of the gate dielectric film of Bai as is taught by Pomarede because Pomarede teaches that it is advantageous to treat the surface of a layer that will have an ALD subsequently deposited thereon.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (US 6,166,417) in view of Chang et al. (US 6,660,630).

Regarding claim 39, Bai does not disclose depositing a layer of conductive material over the first and second gate electrode layers. However, as is discloses by Chang, it is necessary in the fabrication of semiconductor devices such as that of Bai, to deposit multi-layered conductive interconnection structures above the gates of a semiconductor device in order to provide required wiring to the gates of the device (col. 1, ln. 34-65). Such structures are well-known in the art. At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit conductive material over the first and second gate electrode layers of Bai for the purpose of forming a multi-layered interconnection structure that connects the gate with upper-level wiring because such structures are necessary to the function of the gate and are well-known in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

CLN
January 26, 2004

Michael Trinh
Primary Examiner
Act SPE
1/26/04